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#12

ON THE

PHYSICAL REALIZATION OF AN

ELECTRONIC COMPUTING INSTRUMENT

BY

Julian H. Bigelow

Herman H. Goldstine

Richard W. Melville

Peter Panagos

James H. Pomerene

Jack Rosenberg

Morris Rubinoff

Willis H. [illegible]

The Institute for Advanced Study
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PREFACE

This report constitutes the fifth in our series of interim progress reports and covers the period from July 1, 1948, to December 31, 1948. It is prepared in accordance with the terms of Contract W-36-034-ORD-7481 between the Government of the United States and The Institute for Advanced Study.

In our four previous reports we have attempted to describe in considerable detail the underlying principles and criteria upon which the various organs would be designed. Work has now progressed to the point where much of our preliminary studies has been translated into engineering realities. Therefore our present report reflects this change in emphasis. The design considerations which influenced the choice of the circuits used in, for example, the adder, are those described in the previous reports. Therefore more and more our newer reports will describe the exact workings of our circuits and their final performance characteristics rather than the basic motivations.

All the engineering work here is under the direct supervision of Mr. Julian H. Bigelow, our chief engineer. His engineering staff consists of four electrical engineers, Messrs. J. H. Pomerene, J. Rosenberg, M. Rubinoff, and W. H. Ware, and of two mechanical engineers, Messrs. R. W. Melville and P. Panagos.

Herman H. Goldstine

1 January 1949

CHAPTER I

THE MEMORY ORGAN

1.1 Introduction. Of the four basic organs comprising our computing machine perhaps the most critically difficult one, from an engineering point of view, is the memory organ. At the present time there are three main directions in which various engineering groups are moving in an effort to find an adequate memory organ for a high speed digital computer. These three developments are 1) the mercury delay line, 2) an electrostatic storage tube, and 3) a magnetic drum. Of the three our group has concentrated its attention on the latter two, and we shall describe below our work along these two directions in some detail

From our experience with coding of problems we are of the opinion that the high speed memory of a reasonably well-balanced computing instrument should have a capacity of at least 1000 words -- by a word we mean a set of 40 binary digits -- and should be capable of functioning at electronic speeds. The exact functions of the memory organ must be to receive information from other parts of the machine, to hold that information until it is needed later in a calculation, and finally to transmit upon command that information to other parts of the machine. It is quite desirable in this connection that the memory be such that the act of transmitting an item from it does not erase the item. Finally the functions of receiving and of transmitting or "writing into" and "reading out" must be performed at rates which are in balance with the other parts of the computer. Since we plan a multiplier capable of operating somewhere between 2,000-4,000 times per second we want the reading and writing time for the memory to be in the range 10-50 μs.

Of the three types of memory organs now under development only the second one, the electrostatic storage tube, is capable of operating in the frequency range just mentioned, i.e. 10-50 μs. The mercury delay line operates in the range 500-1000 μs, and magnetic drums are perhaps a factor 5-10 slower than this.

At the present time there are to our knowledge four more or less different approaches to the electrostatic tube: the so-called Williams tube named after its inventor Professor F. C. Williams of the Victoria University in Manchester, England; the RCA Selectron which, at the time of writing this report, has nearly been completed by its inventor Dr. Jan Rajchman; the Whirlwind tube being developed at MIT under a classified contract with ONR; and the so-called Haeff tube named after its inventor Dr. A. V. Haeff of Naval Ordnance Laboratory. This tube was invented for a different purpose from computers, and the National Bureau of Standards is undertaking a project to adapt the tube to computer use.

Early this summer we became aware of Professor Williams' work and learned of the very advanced stage of his development. We felt that this tube gave substantial promise of being an excellent answer to the memory problem for our machine and that it certainly should be studied with the greatest care. From our point of view it had the highly desirable feature of using only conventional cathode ray tubes and vacuum tubes whereas the other three developments all centered around specially designed tubes. Since we are unequipped to undertake tube developments we felt that in the cases of the Selectron, the Whirlwind, and the Haeff tubes all we could do is to watch their progress with keenest interest. In the case of the Williams tube, however, the entire problem was one of circuit design and construction, fields in which we feel competent. Accordingly we decided

without prejudice to our whole-hearted interest in the Selectron, to undertake a critical investigation of Williams' work.

To this end our chief engineer, Mr. Julian Bigelow, went to England to confer with Professor Williams, and Mr. James H. Pomerene, another of our engineers, started a development of circuits to modify for our use. Williams himself had devoted most of his interest to the use of his tube as a serial memory although he makes mention of the feasibility of its use as a parallel memory, which is what we desired.[1)]

In a matter of about six weeks Pomerene had a somewhat crude circuit assembled which was sufficiently reliable, however, to enable him to store a pattern of 256 binary digits. After making quite thorough tests with this preliminary circuit, he felt it worth our while to design refined circuits and to carry out an extensive development. This latter work is now underway and will be described in our report next July.

As was mentioned above we are also carrying on a small development program with respect to magnetic drums. This work was initiated under a contract with the Office of Naval Research and has been continued since the expiration of the Navy contract on June 31, 1948. In order to give a coherent account of our investigations during the period covered by this report we have appended to this report our final report to ONR. Speaking broadly, we have been engaged since July in constructing and testing, with a somewhat low priority, a drum of the sort described in our ONR report. Dr. M. Rubinoff is the engineer in charge of this program.

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1) Cf. F. C. Williams and T. Kilburn, A Storage System for Use with Binary-Digital Computing Machines, Institution of Electrical Engineers, Nov. 1948; Pt. III, March 1949 . In what follows we give in effect a brief account of some of the results described in this paper.

The principal reason we are concerned with the magnetic drum lies in our need for a memory of about 1000 words and in our uncertainty whether an electrostatic storage tube can at present be built with that capacity. If it should turn out that an electrostatic memory is capable of storing, say 256 words, then a magnetic drum could be used as a subsidiary memory with a capacity of about 1000 words.

In Secs. 1.2-1.5 below we describe in some detail Williams' very elegant results; in Secs. 1.6-1.9 we discuss our results on the Williams tube; and in Section 1.10 we discuss our work on the magnetic drum.

1.2 A Description of Williams' experiments. In the Williams tube information in binary form is stored by charge distributions in the phosphor coating on the inside of the tube's face. A screen of fine wire is attached directly to the outside of the tube's face. Thus the part of the phosphor containing the various charge distributions is capacitively coupled to the wire screen, and it is then possible by focussing the beam at a given point to produce a signal on the wire screen.

To understand the physical principle underlying Williams' experiment we recall the well-known secondary emission property of dielectrics. If we plot the ratio of secondary to primary electrons against the velocity of the primary electrons when the substance is phosphor then for a considerable velocity range -- probably several thousand volts -- the ratio is above 1. Thus if a beam of suitably high velocity -- in the order of 1-2,000 volts is focussed on a spot on the phosphor coating a positive charge will result at the given spot since more electrons are leaving the phosphor than are being deposited. Thus the potential of the spot will rise above the

potentials of all electrodes in the tube; this will then result in a situation where some secondaries will return to the spot and others will move into the neighborhood of the spot. Finally a steady state situation will be reached with respect to potential at which the effective ratio of secondary to primary electrons is 1. After this point is reached the given spot will remain constant in potential, but the size of the spot will swell and encompass a larger area of the screen. According to Williams, if the beam is left on for less than 400 us the screen is not affected at distances greater than a spot diameter.

In Figure 1.1 below we give a picture of the positive charge distribution as a function of distance assumed in the phosphor by turning the beam on a spot; in this sketch the dotted lines show the extremities of the beam. If now a second spot is formed on the phosphor quite close to the first one -- not farther away than 1.33 spot diameters -- then some, at least, of the secondary electrons given off in the formation of the second spot are attracted to the positively charged area of the first spot with the result that the first spot will be partially filled in.

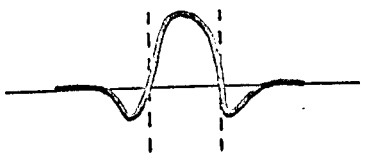


Figure 1.1

In Figure 1.2 below we give a picture of the charge distribution as a function of distance assumed by two dots close together, the dotted lines defining the extremities of the two dots.

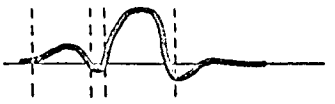


Figure 1.2

Next, let us discuss the behaviour of the wire screen on the face of the tube. To make our future discussion somewhat simpler from a notational point of view we shall call a single spot a dot or a 0 and a closely coupled pair of a continuum of spots a dash or a 1. Let us first consider what happens when the beam is suddenly turned on. Since the phosphor screen and the wire screen are capacitively coupled, the effect of the beam turn on is to induce momentarily in the wire screen a positive charge; if this latter screen is then connected to ground via a resistance, a transient current will flow to the wire. Again when the beam is cut off sharply an opposite current will flow. We illustrate the situation in Figure 1.3 below,

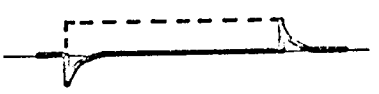


Figure 1.3

where the dotted line indicates the square wave used to turn the beam on. If the place at which the beam was turned on was a dot, then there is no further current flow and hence no further output signal. If, however, the place was a dash, then two other signals are emitted: first, the beam will rapidly "dig" electrons out of the phosphor and thereby establish a flow of current out of the wire screen, and second, the electrons leaving the "hole" that is being dug will fill in the "hole" next to it thereby causing a flow of current into the wire screen. We reproduce below the essentials of Williams' graph of these three effects in Figure 1.4.

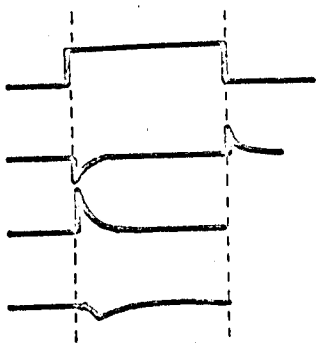


Figure 1.4

In this figure, (a) represents the square wave used to turn the beam on and off; (b) represents the transient caused by turning the beam on and off and thus (b) corresponds to Figure 1.3; (c) represents the signal emitted as a result of "digging" out electrons; and (d) represents the signal emitted as a result of "filling" in the neighboring hole. The signal (d) does not have as sharp a wave front as does (c) since the filling in process takes place more slowly than does the excavating process and (d) has a smaller amplitude than (c) since the filling in is not as complete as is the excavation.

These things being understood we then see that the output signal for a dot is as illustrated in Figure 1.3 and for a dash is the sum of signals (b), (c), and (d) in Figure 1.4, i.e. as given by Figure 1.5 below.

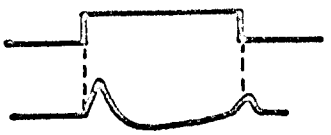


Figure 1.5

It is possible to change the amplitude and even the polarity of the signal in Figure 1.5 by properly adjusting the brightness and focus.

We are now able to describe the processes of writing a 0 or a 1 at a place in the tube, of reading what is stored at a given place and of "regenerating" what is stored at a given place.

From what we have seen earlier when the beam is turned on a dot a signal of one polarity is emitted and when turned on a dash a sign of the other polarity is emitted -- we disregard all except the leading pulse in each case. Thus we have a mechanism for reading. As we have described this mechanism the act of reading a dot will not destroy the dot but will in fact serve to regenerate it. In fact, if some electrons had leaked into the "hole" defining the dot the effective secondary to primary ratio at that place would be slightly above 1 and the beam would therefore "dig" the extra electrons out thereby restoring the original configuration. Thus

the act of reading a dot will regenerate it. Williams has measured the leakage time constant of some phosphor and finds it is about 0.2 seconds. If then each dot is read at least once every 0.1 seconds, then it will be permanently stored.

As we have described the reading of a dash above the process would effectively convert the dash into a dot. If the dash is a pair of closely coupled dots then it suffices after reading the dash to move the beam to the proper position and to write there another dot. If the dash is a continuum of dots it suffices after reading the dash to leave the beam on and to move it across the proper distance. In either case we have called the small beam displacement needed a "twitch". Thus, if we connect the output of the wire screen, or rather the output of the video amplifier which amplifies to a usable level this output, to a "twitching" circuit in such a way that a dot renders the "twitch" inoperative and a dash activates it, then we have not only a complete mechanism for reading but also for regenerating either a dot or a dash provided only that each character stored is regenerated at least every few tenths of a second.

To recapitulate: When a dot is read or regenerated the output of the amplifier is used to hold the beam on the dot and to turn off the beam. When a dash is read or regenerated the output of the amplifier is used to hold on the beam and to "twitch" it.

Finally, we describe the writing process. We have in effect already described how to write a dot or dash upon a place where there is no prior charge distribution or where there is already a dot or dash, respectively. To change a dot already stored into a dash is also trivial. It remains only to describe how to write a dot upon a place where a dash is

stored. To accomplish this the beam is turned on, and electrons are dug out which partially fill the other dot of the dash. Now when the beam is again turned on this place to read or to regenerate the signal the output pulse will be that corresponding to a dot and the beam will be turned off. With time leakage will gradually fill in the small hole.

Since Williams uses his tube as a serial device and we use it as a parallel one, we do not continue further our description of his apparatus. However, it is worth remarking that he used an area 8 cm x 12 cm on a 6 inch cathode ray tube for storing 1024 binary digits.

1.3 A Description of the Institute Experiments. Preliminary remarks. We go now to describe the preliminary work done by Mr. Pomerene in modifying for parallel operation the Williams tube. Williams arranged his apparatus in such a way that he could for purposes of reading or writing, deflect the electron beam to any horizontal row and then serially read the 32 digits stored on that line. Pomerene instead wished to deflect his beam both horizontally and vertically to any given place on the tube face and then read or write there. Furthermore Pomerene used various 5 inch cathode ray tubes instead of 6 inch tubes as did Williams.

Pomerene's program necessitated using different circuits from those used by Williams, and we describe them below. It should be borne in mind that this equipment was not intended as a final solution but should rather be viewed as an attempt to establish a principle and to verify Williams' results. In our next report we shall describe the refined circuits subsequently designed by Bigelow and Pomerene.

On succeeding pages we give five circuits, Figures 1.6-1.12 which contain the essentials of Pomerene's equipment. We first describe these circuits and then discuss his experimental results.

Pomerene like Williams decided to regenerate the places in his array serially. Unlike Williams he decided to arrange his time cycle in the following way: Let τ be the number of microseconds required to read, write, or regenerate a single place in the array and let N be the total number of places in the array. We call the time interval τ a cycle. During each even cycle a point of the array is regenerated; this regeneration routine is carried out in a linear fashion, an electronic counter being provided to remember which place was regenerated in the preceding even cycle. During each odd cycle it is possible to deflect the beam to an arbitrary place for the purpose of reading or writing. Thus 2N cycles are required to afford a complete regeneration of all places in the stored array. Of these cycles 50% are available for reading or writing while the remaining cycles are, from the point of view of the logical use of the memory, wasted.

In order to remember what place in the array was regenerated last and to change by one each time this place designation we need a counter, one stage of which is shown in Figure 1.6. To remember whether the equipment is in an even or odd cycle we need a binary device such as a toggle. This is also shown in Figure 1.6. The even cycles are called regeneration cycles and the odd cycles action cycles. To store the place at which an action will occur we need a register. This is shown in Figure 1.7. To deflect the beam to the proper place we need some sort of deflection circuit which can change a digital quantity -- the output of the counter or the register -- into a voltage level. This unit, shown in Figure 1.8, is called a deflection

adder. Finally we need a clock for emitting the proper sequence of pulses and a gate circuit for controlling the operations of the other circuits. These are shown in Figures 1.9-1.11 and the video amplifier in Figure 1.12.

1.4 A Description of the Institute Experiments. The Counter. The circuit diagram, Figure 1.6, shows the so-called 0-th stage of the counter associated with the regeneration cycle. In all the counter contained 11 stages, 0-10, of which 1-10 were identical. Stage 0 differed in that it was used to decide whether an action or regeneration cycle was to be performed. As a result it contained a voltage divider network not present in the other stages. This divider can be seen in Figure 1.6 leading out on a lead for choosing between regeneration and action cycles.

Before describing in detail the action of this counter we wish to stress that it was intended as a purely interim device which has since been abandoned.

The two halves of the 6J6 are interconnected to form a flip-flop which can be controlled by one of two different gating circuits. The input lead to each stage is the one marked "dash end"; in the case of the 0-th stage there is a pulser to feed this bus whereas in the other stages the output pulse of the preceding stage is fed into this bus. Thus the system is degenerative in character, which is of course not wholly desirable. The dash end bus in its quiescent state is at +100 volts and when pulsed rises momentarily to +180 volts. The plates of the flip-flop are at one or the other of the levels +190 volts, +120 volts and the ungrounded grid of this flip-flop is at either +20 volts or -20 volts.

To explain the action of the counter stage let us consider how it acts under the influence of a pulse at the input bus.

First, let us assume that the left half of the flip-flop is conducting. Then the corresponding plate is at +120 volts and the other plate is at +190 volts with its grid at -20 volts. Thus the suppressor grid of the 6AS6 is also at -20 volts and its plate is at +120 volts as is the cathode of that half of the 6AL5 in the plate circuit of the 6AS6. Also the grid of the half of the 12AT7 connected to the plate of one half of the 6J6 is at +190 volts, which causes the top of the 56 k resistor in the cathode circuit to be at +190 volts, hence the cathode of the associated 1N38 to be at the same potential. (It should be remarked that in designating the two elements of a crystal, contrary to the present terminology, we used a triangle to stand for the G3 element and a bar to stand for the "cat's whisker".) The other half of the 12ATL is so arranged that normally the cathode and grid are at +100 volts. Now when a pulse is applied to the "dash end" or input bus, two things result: On the one hand the cathode of the 1N38 in the input circuit rises to +180 volts and since the cathode of the other 1N38 is at +190 volts the grid of the associated half of the 12AT7 rises and the cathode uses accordingly thereby sending an output pulse to the next stage of the counter and also raising the plate of that half of the 6AL5 connected to the 6J6. Thus the plate of the 6AS6 is raised to +190 volts and the left-hand plate of the 6J6 is also raised to +190 volts, thereby starting to flip the flip-flop. Concurrently the pulse on the cathode of the 6AL5 raises the grid of the right half of the 6J6 to help throw the flip-flop into the opposite state. Then about 1.5 us later the RC-delay line connecting the grid of the right half of

the 6J6 to the suppressor grid of the 6AS6 will allow the latter grid to rise to +20 volts. Before this can happen, however, the input pulse has passed through the 1000 μμf condensor into the cathode of the 6AS6. It is not able to place the 6AS6 in a conducting state and therefore nothing further happens.

To summarize: If the flip-flop contains a 1 and if the stage is pulsed, then the flip-flop is put into the opposite state, and a pulse is passed into the succeeding stage. The static output lead marked "Out to Gates" is put at +20 volts and in the 0-th stage the special output lead is put at -20 volts.

Second, let us now assume that the left half of the flip-flop is not conducting. Then the plate of the 6AS6 is at +190 volts and its suppressor grid is at +20 volts. Thus this gate is now open to pass through its plate a pulse which will reverse the state of the flip-flop. The half of the 12AT7 connected to a plate of the flip-flop is now so biassed that its cathode is at +120 volts,and therefore the 1N38 in its cathode circuit has its cathode at +120 volts. Thus a pulse on the input bus will not be able to bring the grid and hence the cathode of the other half of the 12AT7 high enough to emit a signal, and no output pulse will be sent into the next stage.

To summarize: If the flip-flop contains a 0 and if the stage is pulsed, then the flip-flop is put into the opposite state and no pulse is passed into the succeeding stage. The static output lead is put at -20 volts and in the 0-th stage the special output bus is put at +20 volts.

Finally it remains to explain the function of that half of the 6AL5 in the grid circuit of the 6AS6. This tube is intended to prevent the grid in question from going below -20 volts. Such a device is needed because at a high duty cycle the 1000 $\mu\mu$f condensor may change the grid level by not discharging completely.

1.5 A Description of the Institute Experiments. The Action Regeneration Gates and the Register. There are ten register stages and ten action-regeneration gates of which one of each is shown in Figure 1.7. The grids of the 12AT7 are connected to the two static output leads of the 0-th stage of the counter. If the figure shows the n-th register stage and the n-th gate (n = 1, 2, ..., 10), then the static output lead of the n-th stage of the counter is introduced into the gate at the point marked "Gate signal from counter (Stage n)".

First, consider a regeneration cycle, i.e., let the 0-th stage of the counter contain a 0, i.e., the left half of the flip-flop in the counter stage is not conducting. Then as we say in 1.4 the regular static output of the stage is at +20 volts and the special 0-th stage output lead is at -20 volts. (Cf. the voltage levels indicated in the upper right-Hand corner of Figure 1.7.) We assume the regular static output of the 0-th stage is fed into the left grid of the 12AT7 and the special output into the right hand grid. Thus the corresponding cathodes are at +20 volts and -20 volts, respectively, and this puts the appropriate grids of the two 6J6's at +20 volts and -20 volts. The left hand 6J6 is now such that its cathode will be at the higher potential of its two grids; since the output of the register stage is $\pm$ 20 volts, this cathode will be at +20 volts. Again the cathode of the right hand 6J6 will be at the higher potential of its two grids; since the gate signal from the n-th stage of the counter is

+20 volts and since one grid is in the present case at -20 volts, the cathode of this 6J6 will be at the same level as the static signal from the n-th counter stage. The two Ge crystals are so arranged that their common anode is at the smaller of the potentials of the 6J6 cathodes. Thus this point will be at the same potential level as the static signal from the n-th stage of the counter. There is attached to the bus leading from this point a diode which is intended to standardize the upper level, which would normally be +20 volts, to +15 volts.

Second, consider an action cycle, i.e., let the 0-th stage of the counter contain a 1, i.e., let the right half of the flip-flop in the counter stage be not conducting. The static output levels of the 0-th stage are reversed and thus the cathode of the right hand 6J6 is at +20 volts irrespective of the counter signal from the n-th stage. Also the potential level of the left hand 6J6 is determined by the state of the register 6J6. (This is so arranged that when the left half of the register flip-flop is conducting, the output level is -20 volts and is +20 volts in the other case.) Thus by a discussion of the sort we made above the level at the point where a signal is sent to the adder is +15 volts or -20 volts according as the output of the register is +20 volts or -20 volts.

To summarize: In an action cycle the output of the counter is disconnected and according as the proper register stage is a 1 or a 0 a voltage is applied to the adder of -20 volts or +20 volts. In a regeneration cycle the output of the register stage is disconnected and according as the proper counter stage is a 1 or a 0 a voltage is applied to the adder of -20 volts or +15 volts.

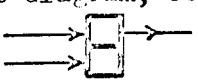
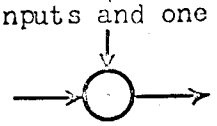
The register consisted of a flip-flop per stage of exactly the same design as used in the counter. As is indicated in Figure 1.7 it could be manually set by a toggle switch in one of the grid circuits.

1.6 A Description of the Institute Experiments. The Deflection Adder. In Figure 1.8 is shown the five-stage deflection adder used for applying the proper voltages to the horizontal plates of the cathode ray tube. A similar adder was used for vertical deflection except that the twitch and dot-dash differential circuits were lacking.

As is seen from Figure 1.8 there are five 6J6's with one grid of each tied to ground and with the other grids tied to leads from the appropriate stages of the action-regeneration gates. All plates of the right hand and left hand halves of these 6J6's are tied respectively in common. The cathode resistors are so arranged that when conducting the current flow through each tube are as 1 : 2 : 4 : 8 : 16 with the most current flowing through the fifth stage — this was about 10 ma. These currents are summed in the two resistors connected to +300 volts, and the resultant voltage is applied to the appropriate deflection plates.

In the horizontal deflection adder the dot-dash differential and twitch circuits also control the deflection voltages as follows: In the lower right hand corner of Figure 1.8 we show the shapes of the dot, dash, and differential output pulses. The 12AT7 is so biassed that in its quiescent state the grid connected to the dot bus is at +20 volts while the dot bus is at -20 volts. The dash bus holds the other grid at -20 volts. Thus normally the right half of the 12AT7 is conducting, and its plate is at +120 volts while the other half has its plate at +190 volts. Also the right hand grid of the 6J6 in the twitch circuit is at -15 volts and the 1N34 crystal will prevent it from going above +15 volts.

Since the twitch, i.e. the horizontal deflection which distinguishes a dash from a dot, is to take place just after a dot has been turned off and is to last until the end of a dash, both the dot and dash pulses are simultaneously applied to the appropriate grids of the 12AT7 as indicated in the figure. The leading edges of both pulses occur simultaneously and therefore the state of the 12AT7 -- the right half conducting -- is not disturbed until the trailing edge of the dot pulse is reached. At this time the situation is altered and the right half is turned off. Thus its plate rises to +190 volts and the right hand grid of the twitch 6J6 rises to +15 volts which causes the plate of the left half of the same 6J6 to fall, thereby applying a voltage change to the horizontal deflecting plates, which lasts until the end of the dash pulse.

1.7 A Description of the Institute Experiments. The Gate Circuit and the Clock. In Figure 1.9, 1.10, we show a block diagram of the gating circuit and a detailed circuit diagram, respectively. In the block diagram a pair of rectangles, sic  is used to indicate a flip-flop with two inputs and one output. A circle with two inputs and one output, sic  is used to indicate a gate circuit. It is assumed that these elements preserve the polarity of the input signal. Finally a lead with an open arrow ⟶ is used to indicate a lead carrying a pulse and lead with a closed arrow ⟶ a lead carrying a gate signal.

In Figure 1.9 we see the block diagram. In the upper right hand corner we have indicated the various clock pulses and gates available. These have the following functions:

1) We note in Figures 1.3 and 1.5 that at the beginning of a dot or a dash a pulse is produced of opposite polarity in the two cases. The strobe is a pulse which occurs during the first phase of a dot or a dash.

2) During each regeneration cycle a signal of +20 volts is produced; this is the regeneration gate signal.

3) During each action cycle the regeneration signal is cut off and a signal of -20 volts is produced; this is the action gate signal.

4) During each cycle, whether action or regeneration, three signals -- a dot pulse, a dash pulse, and a dash-end pulse -- are produced.

In the upper left hand corner is one deck of a two deck, three position manual switch. If it is set to read a dc level of +20 volts is applied to the gate tube, 1. If it is set to either T or H, this gate is open during a regeneration cycle and is closed during an action cycle. If it is set to read, this gate is always open. When gate 1 is open, a dash output and only a dash output from the amplifier will allow a strobe pulse to set the indicated flip-flop I -- it is reset by the dash-end pulse, as indicated. If this flip-flop has been set, it opens gate 3 and allows a dash signal to reach the gate 4 -- also a dot will always reach this gate. If a regeneration cycle is on, then gate 4 is open and the dash will be applied to turn on the beam of the cathode ray tube. If the dot output of the amplifier was a dot, then clearly a dot was applied to turn on the beam.

The amplifier output is also routed to gate 7 which will pass a strobe pulse if and only if the amplifier output is a dash. This pulse then tries to proceed through gate 6 and set the read toggle, flip-flop II. We now discuss the other input to gate 6.

Flip-flop III is controlled by a manual push-button, as indicated in the figure. If III is set, gate 8 is opened and during a regeneration cycle the dash-end pulse H_t passes through 8 to set flip-flop IV. During an action cycle, H_t gets through 10 to reset IV. When IV is changing to the "set" state it emits a pulse which acts to reset the read toggle II, tries to set toggle I, and also resets III; the latter occurring if and only if the indicated second deck of the switch is set to H, i.e., to dash. As soon as the flip-flop IV has come to a steady state gate 6 is opened via gate 6, and the read toggle is free to assume the state dictated by the amplifier output. Thus the information stored in the tube is transferred into a flip-flop memory.

The setting of IV also opens gate 5 and allows during either the H or T pulse to be applied to the cathode ray grid when a regeneration cycle is not on and hence when gate 4 is closed.

To summarize: If the 2 gang, 3 position switch is set to T or H, then the output of the amplifier is used to turn on the electron beam either for a dot or a dash according as the amplifier output is a dot or dash. If the switch is set to read and the push button pressed the amplifier output is put into the read toggle.

With this explanation in mind one can then easily verify that the circuit of Figure 1.10 performs the functions just described.

Figure 1.11, a schematic of the clock, is essentially self-explanatory, and we say no more of it at this time.

1.8 A Description of the Institute Experiments. Summary of Results.

By mid-September Pomerene had reached the following operational conclusions:

1) A stable pattern of 32 points on a line had been obtained with regeneration frequencies from 100 cps-100,000 cps. At a lower rate 32 cps -- each spot regenerated every two seconds, since an actioncycle always followed a regeneration cycle -- the operation was not wholly reliable.

2) When a full pattern of 1024 points on the screen was used, the extremities were not completely stable, and the dot position in these regions was apparently affected adversely by hum and pickup in the supply lines. With the present circuit a somewhat smaller pattern was stable -- since the counter is binary, this smaller pattern consisted of 256 points.

3) The counter was not wholly reliable.

It was felt this fall that our group had verified quite completely Williams' experiments and that further significant advances were not possible without radical improvements in our circuits. Accordingly a careful redesign study of the circuits associated with our Williams tube was begun. Since this work is preliminary to the actual design and construction of new, reliable circuits, which took place after January 1, 1949, we postpone until the next report a discussion of this work by Bigelow and Pomerene.

1.9 A Description of the Institute Experiments. Phosphor Studies.

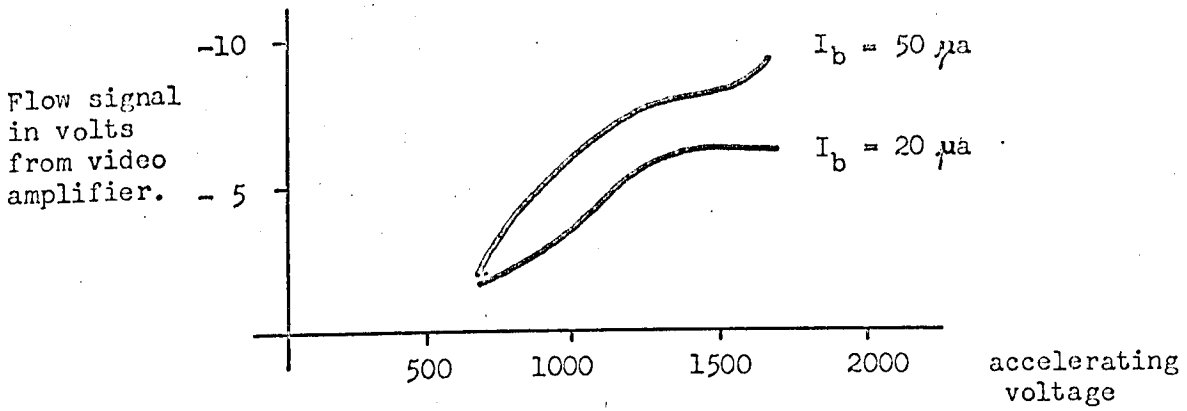
Williams had made a number of studies of the effect on storage of imperfections in the phosphor coating of a cathode ray tube which Pomerene has verified. Also Pomerene made a number of additional studies of the problem.

According to Williams there are three major sources of imperfections in the phosphor coating of a tube: carbon specks on the phosphor, impurities in the phosphor, and minute holes in the phosphor. The reason these may cause difficulties is that the impurities -- the hole is in a sense also an impurity since the glass tube face then acts as the dielectric -- have a secondary-primary electron ratio usually less favorable than the comparable ratio for the phosphor itself, i.e., the ratio for carbon is always less than unity and for glas it drops below unity before it does for the phosphor. Thus bombardment of a point with a beam of sufficient velocity can result in forming a negative charge distribution at the point and thus make it impossible to store a dash.

Bigelow devised a simple means for visually examining the face of a cathode ray tube which proved quite helpful. The method is very similar to one used by S. Alexander of the National Bureau of Standards for a comparable task. The method consists of sweeping the face of the tube in question by a raster of the sort commonly used in television and simultaneously sweeping a viewing tube with the intensity of the beam of the second tube modulated by the amplifier output of the first or Williams tube. In this way irregularities in the amplifier output appear as abnormally bright or dark spots on the face of the viewing tube. Figure 1.12 is a photograph of such a pattern.

Both Williams and Pomerene discovered that as the accelerating voltage is diminished the importance of an imperfection is diminished. For a 5JP1 tube Pomerene ran some tests to measure the flow signal voltage output for a constant beam current as a function of accelerating voltage.

With constant writing rate and with beam currents of 50 μa and 20 μa, respectively the results are roughly as follows:



The dot output signal from the amplifier over the range from 800-1600 of accelerating voltages is of the order of +6volts, +5 volts and the dash output about -10 volts, -5 volts for beam currents roughly comparable to the conditions shown in the two graphs above.

1.10 The Magnetic Drum. There is attached hereto as an appendix a very complete report describing work done at the Institute on the development of a multi-channel magnetic drum memory under Contract N6-ori-139, Task Order II, which terminated June 31, 1948. Since that date Dr. Rubinoff has continued this work in order to explore quite fully the potentialities of magnetic drum memories. The reason for appending the report to the Navy is for the purpose of completeness in this series of reports to the Ordnance Department.

Since July 1, Rubinoff has studied three different types of magnetic coatings for drums and has begun various tests to determine a material most suited for his application. The materials used are:

a) A nickel plating, .0003 in. thick.

b) A nickel plating, .0007 in. thick.

c) A nickel-cobalt alloy, .0007 in. thick, made by the Brush Development Company.

d) A suspension of iron oxide furnished by the Minnesota Mining Company.

Of these four coatings the last one has the considerable virtue that a drum can be coated by spraying techniques in almost any shop whereas the other coatings require very special apparatus and techniques not found in most laboratories. The experiments to date do not show coating d) to be substantially different as a magnetic medium from a) - c).

A drum coated with iron-oxide was fabricated and mounted together with a set of reading-writing heads, as described in the Appendix, and tests were started. Rubinoff is at present confining his investigation to only one or two heads for the purpose of getting performance characteristics of each channel and of studying possible interference between adjacent channels.

Quite preliminary measurements and tests have been made with this drum and these are given below. It is however worth emphasizing that the results stated below are still very preliminary and are useful only in indicating orders of magnitude.

The reading-writing heads are separated by 1/4 in. between centers, and the magnetic charges they deposit are separated from each other by about 1/16 in. No interference is observed between adjacent channels.

With data stored on a channel, the drum was originally run at 1000 in, per second and measurements were made at this speed. However, since then it has been running at 2000 in. per second. The output signal has a peak voltage of about 100 μv, and the pulse is about .2 μs in duration. The output voltage is proportional to the speed of rotation. The pulses read of the drum were in the main put on the drum while it was stationary and consisted of a current pulse of about 10 a for about .2 μs.

There is a very considerable amount of energy stored in each magnetic pulse; in fact, it is entirely possible to feed the output of the reading-writing head directly into a transformer and to produce voltage amplifications of the order of 100-200 times. The most critical part of Rubinoff's investigations to date has been to determine the characteristics for this transformer. For the greater the amplification we can secure in this manner by a pulse transformer the less is required in the way of an amplifier. It is hoped that a one-tube amplifier per channel will suffice, but it is still too soon to know.

It is hoped that definite specifications for the transformer can be determined upon in the near future so that this development can be completed.

CHAPTER II

THE ARITHMETIC ORGAN

2.1 Introduction. In our fourth interim report there is a detailed discussion of the shifting registers, which were given their life and performance tests during the present time period. For details of the design and construction of these registers the reader should consult the fourth report, Chapter III. We give at this time the performance characteristics.

Since the writing of the last report the circuits and design characteristics for the adder were decided upon and the units themselves built and installed. Also both static and dynamic tests were made on the unit, which we give below. These tests are not complete since the gate circuits for controlling the flow of information between the registers and the adder were not complete as of January 1.

The detailed test results are given below, but it is perhaps appropriate to remark that they are entirely satisfactory and indicate that the major portion of the arithmetic organ is completed.

The tests and work described below have been and are continuing to be the joint responsibility of Messrs. Rosenberg and Ware.

2.2 The Adder. In Figure 2.1 below we give a circuit of the adder showing two stages. Before describing in detail the operation of the circuit we first discuss in more general terms its mode of operation. It is also well to once more emphasize at this point that the same principles of circuit design, which motivated the design of the shifting registers, have been embodied in the adder.

Since the arithmetic organ is to be a 40-stage "parallel type" one, the adder contains 40 essentially identical stages each of which has three inputs and two outputs. In our so-called "one-address code" we presuppose that in an addition the augend is already in the accumulator register and the order for an addition consists of transferring the addend into the memory register and forming the sum. The digits of the augend are indicated in Figure 2.1 as the resident digits and those of the addend as the incident digits. The latter are transferred into the adder via the so-called complement gates, which allow a number or its complement to be sent into the adder. The result of the addition, the sum, is transferred out of the addder via the so-called digit resolver gates. At the time of writing neither the complement nor digit-resolver gates have been completed in their final form.

Each stage of the adder has three inputs, one for each of the resident digits, the incident digits, and for the carry digit from the preceding stage. There are two outputs, one for the carry digit and one for the sum digit. The adder itself is of the so-called "Kirchoff" type as distinguished from the types of adders using only gate tubes. The full implications of this will be better understood as we explain in detail the functioning of the adder.

Let us consider the stage of the adder shown in the left half of Figure 2.1. It consists of the three 6J6's, numbered 1, 3, 4, the left half of the 2C51, numbered 2, and the left half of the 2C51, numbered 5. We shall call the left half of tube n n.ℓ and the right half n.r.

In principle it operates as follows: We bring to a summing resistor the carry digit from the previous stage as a unit of voltage, and the resident and incident digits as units of current. The sum of these three quantities 0, 1, 2, or 3 voltage units is now applied as a grid bias to a gate which is so arranged that it discriminates between the cases (0, 1) and (2, 3) giving out a voltage unit only in the latter case. This is, of course, the carry digit. The sum of the three input quantities is also fed into the so-called digit resolver which is a set of gates that decide whether the sum is either one of (1, 3) or or (0, 2). In the former case, the unit digit of the answer is a 1 and in the latter it is a 0. This result is then fed into one half of the augend register displacing what was there. The digit resolver circuit will be discussed in our next report and is not shown in Figure 2.1.

The cathode follower 2.χ has as its cathode load the 10.5 k summing resistor and the plates of 3.r and 5.χ in parallel. If the resident or incident digit is a 1, then and only then 3.r or 5.χ is conducting and current flows through the 10.5k resistor. The unit of current corresponding to either tube can easily be seen to be 5 ma. Thus either 0, 5, or 10 ma will flow through tube 2.χ. In the event that the carry digit is a 1, then the grid of 2.χ is dropped by 50 volts. But since a constant amount of current, 0, 5, or 10 ma, is always flowing through a fixed resistor of 10.5k, the cathode point A and the summing point S will then always move together in voltage level; and in the event that the carry digit is 1 both will drop 50 volts. This drop is precisely determined at its bottom level since the tube 1.r is so arranged as a diode that the cathode of 1.r, 1.χ cannot go below the standard level marked E_{01}. It is also fixed at its upper level

since the grid of 1.χ cannot rise above the standard voltage level to which it is tied.

The use of the two cathode followers, 1 and 2.χ, in series is important so that these voltage levels can be accurately maintained. If the carry signal were applied directly to the grid of 2.χ, then grid current would, in certain cases, flow and thus the upper voltage level would be destroyed.

We now see that the summing point S can have any one of four different voltage levels, differing from one another by 50 volt steps. The level of S is applied through an isolating resistor of 22k to the grid of 4.χ. The grid of 4.r is so biassed by the standardized voltage level $E_{01/10}$ that 4.r is normally cut off and only becomes conducting if and only if at least two of the three inputs, the resident digit, the incident digit, and the carry digit, from the preceding stage, are 1. The plate of 4.r which controls whether or not a carry is to be propagated is then tied directly to the grid of the "In" carry cathode follower of the next stage.

The summing point is also connected through a 22k resistor to a tube in the digit resolver, which is not shown in the diagram, where it is decided whether there are an odd or even number of 1's being summed.

To speed up the propagation of a carry a 27 uuf condensor has been used to by-pass the 22k resistor. This allows the carry propagation to get started before a steady state obtains at the point S.

The 47k resistor in the cathode of tube 2.χ is placed there largely to prevent the cathode from attempting to come up toward the plate.

Finally the gate 4 is so biassed that its gating action takes place at the midpoint of the voltage zone of 200 volts, determined by the extreme cases of three zeros and three ones. It should be remarked that small changes in this bias level will affect the rate at which a carry propagates or "collapses" -- this term is used to describe the process of clearing a carry chain out of the adder, i.e., the process of closing all relevant gates 4. Clearly the nearer the bias level of gate 4 is to the boundary of the 50 volt zone determined by three zeros and two zeros plus a one, the more quickly will a carry propagate and the longer will a collapse take.

The operational tests of the adder will be performed during the next period, i.e. after January 1, 1949, but it is of interest to state that the first of these tests showed a carry propagation time of about 6 μs and a carry collapse time of about 5 μs. Furthermore the time to set the gates for an incident or resident digit is about 1 μs. A life test was also performed in which the resident number was fixed at forty ones and the incident number consisted of all zeros except for the last digit which was a one introduced by a pulser. The addition, of course, propagated a carry down all stages and the carry output of the 40th stage was used to trigger the pulser. The test was run for at least eight hours at a repetition rate of about 120 kilocycles per second. No errors occurred during the tests. In the next report we shall describe the further tests of this unit in more detail.

2.3 The Registers. The shifting registers are quite completely described in our fourth interim report. Here we merely give the main results of the tests performed upon them. In order to give an adequate life test to these three registers they were interconnected in two different arrangements to form closed loops of 120 binary digits and shifted a place at a time around the loop.

In the arithmetic organ the registers appear in a vertical plane, one above the other. Let the register from top to bottom be enumerated as 1, 2, 3 as in Figure 2.2.a and Figure 2.2.b.

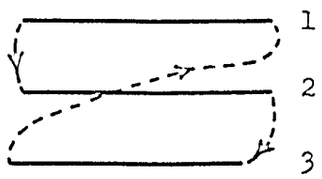


Figure 2.2.a

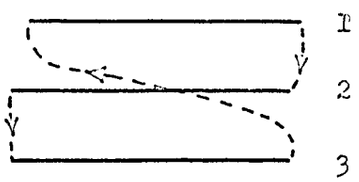


Figure 2.2.b

The arrangement in Figure 2.2.a was used for shifting the pattern to the left and in Figure 2.2.b for shifting to the right.

As was stated in the fourth report a shift consists of two distinct operations: gating the information in one half of a register into the other half and then gating it back again shifted by one place right or left. Each of these operations can safely be performed in 1.5 μs and one can succeed the other with no spacing; thus a complete shift by one place can be safely performed in 3 μs.

At a rate of 3 μs per shift, about 3.3×10^5 shifts are performed per second. At this rate the unit was operated for about 75 hours on left shifts and about 25 hours for right shifts. Thus about 10^{11} shifts in all.

A very extensive set of vibration tests were also made on the registers to find and correct bad solder joints and tubes with defective structures. A number of bad joints were detected, repaired and then no further defects in mechanical structure were found. Also three tubes with defective structures were found and replaced together with two tubes with heaters which burned out. No other tube failures occurred.

APPENDIX

The attached pages contain the relevant engineering data on the work performed at the Institute for Advanced Study for the Navy Department under Contract N6-ori-139, Task Order II. The report was prepared by J. H. Bigelow, P. Panagos, M. Rubinoff and W. H. Ware.